IN THE CLAIMS:

Listing of claims:

1-63. (canceled)

64. (currently amended) A method for forming a semiconductor device including a bonding pad ~~area using a dry etch process~~, comprising:

forming ~~a conducting~~ the pad ~~in electrical contact with an electronic device~~;

forming a silicon oxide layer above at least the pad;

forming a silicon nitride layer above the silicon oxide layer;

~~forming a protective insulation layer on a surface of the conducting pad, the protective insulation layer including at least first and second insulating layers, wherein the first insulating layer and the second insulating layer are formed from materials having different compositions, the first insulating layer comprising a silicon oxide layer, the second insulating layer comprising a silicon nitride layer, the silicon oxide layer being formed on the conducting pad, the silicon nitride layer being formed on the silicon oxide layer;~~

forming a mask above the silicon nitride layer ~~in direct contact with a surface of the protective insulation layer~~ and providing an opening in the mask; and

~~dry~~ etching the silicon nitride layer so that a first aperture is formed in the silicon nitride layer;

etching the silicon oxide layer so that a second aperture is formed in the silicon oxide layer; ~~through the surface of the protective insulation layer at the opening in the mask to form an aperture extending through the silicon nitride layer and the silicon oxide layer to the surface of the pad using CF_4 and O_2 as an etchant, so that the silicon nitride layer includes a side surface surrounding the aperture,~~; and

wherein the silicon nitride layer comprises a side surface surrounding the first aperture, the silicon nitride layer side surface having a tapered shape with an angle in the range of 30 degrees to 60 degrees in relation to a ~~the~~ surface of the ~~conducting~~ pad, and the silicon oxide

layer ~~includes~~ comprises a side surface surrounding the second aperture, the silicon oxide layer side surface having a tapered shape with an angle in the range of 60 degrees to 70~~90~~ degrees in relation to the surface of the ~~conducting~~ pad, wherein the angle of the silicon nitride layer side surface having a tapered shape is smaller than the angle of the silicon oxide layer side surface having a tapered shape.

65. (canceled)

66. (currently amended) A method as in claim 64~~65~~, wherein the ~~dry~~ etching the silicon nitride layer and the silicon oxide layer is conducted ~~includes~~ continuously ~~etching the second insulating layer and the first insulating layer~~.

67. (currently amended) A method as in claim 64, wherein the ~~dry~~ etching the silicon nitride layer includes isotropic etching ~~of at least part of the silicon nitride layer~~ and the etching the silicon oxide layer includes anisotropic etching ~~of at least part of the silicon oxide layer~~.

68-90. (canceled)

91. (new) A method as in claim 64, wherein the angle of the side surface of the silicon nitride layer is in the range of 30 to 40 degrees in relation to the surface of the pad.

92. (new) A method as in claim 64, wherein the etching the silicon oxide layer is controlled so that the silicon oxide layer comprises an exposed upper surface portion, wherein the exposed upper surface portion extends a distance of up to 3 nm between an upper end of the side surface of the silicon oxide layer and a lower end surface of the silicon nitride layer.

93. (new) A method as in claim 92, wherein the etching the silicon oxide layer is controlled so that the exposed upper surface portion of the silicon oxide layer is substantially parallel to the surface of the pad.

94. (new) A method as in claim 64, further comprising:

forming a barrier layer in at least the first and second apertures, the barrier layer being positioned on: (1) the side surface of the silicon nitride layer, (2) the exposed upper surface portion of the silicon oxide layer; and (3) the side surface of the silicon oxide layer; and

forming a bump electrode on the barrier layer.

95. (new) A method as in claim 64, further comprising removing the mask layer after the etching and then heating the device at a temperature of 350°C to 450°C.

96. (new) A method as in claim 95, wherein the heated the device at a temperature of 350°C to 450°C is carried out for a time of 10 to 20 minutes.

97. (new) A method as in claim 64, further comprising forming a polyimide resin layer on the second insulation layer.

98. (new) A method of fabricating a semiconductor device including a bonding pad, comprising:

forming a pad;

forming a protective insulating region on the pad including first and second insulating layers, the first insulating layer being in direct contact with the pad and the second insulating layer comprising being in direct contact with the first insulation layer; the first insulating layer comprising silicon oxide, the second insulating layer comprising silicon nitride;

forming a mask layer on the protective insulating region in direct contact with a surface of the second insulating layer, the second insulating layer being positioned between the first insulating layer and the mask layer, the mask layer including an aperture in a region

corresponding to an electric connection region of the pad; and

dry etching the second insulating layer at the aperture in the mask so that the aperture extends into the second insulating layer;

dry etching the first insulating layer so that the aperture extends into the first insulating layer and contacts the pad;

wherein the etching is controlled so that the second insulating layer includes a side surface surrounding the aperture, the second insulating layer side surface having a tapered shape and including an angle in the range of 30 degrees to 60 degrees in relation to the surface of the conducting pad, and the first insulating layer includes a side surface surrounding the aperture, the first insulation layer side surface having a tapered shape and including an angle in relation to the surface of the conducting pad that is greater than the angle of the second insulating layer side surface.

99. (new) A method as in claim 98, wherein the dry etching the second insulating layer is carried out using an etchant comprising CF_4 and O_2, and the dry etching the first insulating layer is carried out using an etchant comprising CF_4 and CHF_3.

100. (new) A method as in claim 98, wherein, for the first insulating layer side surface, the angle in relation to the surface of the conducting pad of the first insulation layer side surface is in the range of 60 degrees to 70 degrees.

101. (new) A method as in claim 98, wherein, for the second insulating layer side surface, the angle in relation to the surface of the conducting pad is in the range of 30 degrees to 40 degrees.

102. (new) A method as in claim 98, wherein the etching is controlled so that the first insulating layer includes an upper surface portion exposed to the aperture, wherein the upper surface portion exposed to the aperture extends a distance of up to 3 nm between an upper end of the side surface of the first insulation layer and a lower end surface of the second insulation layer.

103. (new) A method as in claim 102, wherein the etching is controlled so that the first insulating layer upper surface portion exposed to the aperture is parallel to the surface of the conducting pad.

104. (new) A method as in claim 98, further comprising:

forming a barrier layer in the in the aperture, the barrier layer being positioned on: (1) the side surface of the second insulating layer, (2) the first insulating layer upper surface portion exposed to the aperture; and (3) the side surface of the second insulation layer; and

forming a bump electrode on the barrier layer in the opening.

105. (new) A method as in claim 98, further comprising removing the mask layer after the etching and then heating the device at a temperature of 350°C to 450°C.

106. (new) A method as in claim 105, wherein the heated the device at a temperature of 350°C to 450°C is carried out for a time of 10 to 20 minutes.

107. (new) A method as in claim 98, further comprising forming a polyimide resin layer on the second insulation layer.

108. (new) A method as in claim 101, wherein, for the first insulating layer side surface, the angle in relation to the surface of the conducting pad of the first insulation layer side surface is in the range of 60 degrees to 70 degrees.

109. (new) A method for fabricating a semiconductor device including a bonding pad, comprising:

forming a pad;

forming a protective insulating region on the pad including first and second insulating layers, the first insulating layer being in direct contact with the pad and the second insulating layer comprising being in direct contact with the first insulation layer; the first insulating layer

comprising silicon oxide, the second insulating layer comprising silicon nitride;

forming a mask layer on the protective insulating region in direct contact with a surface of the second insulating layer, the second insulating layer being positioned between the first insulating layer and the mask layer, the mask layer including an aperture in a region corresponding to an electric connection region of the pad; and

dry etching the second insulating layer at the aperture in the mask to extend the aperture through the second insulating layer;

dry etching the first insulating layer using an etchant comprising to extend the aperture through the first insulating layer;

wherein the etching is controlled so that so that the second insulating layer includes a side surface surrounding the opening, the second insulating layer side surface having a tapered shape and including an angle in the range of 30 degrees to 60 degrees in relation to a surface of the conducting pad;

wherein the etching is controlled so that the first insulating layer includes a side surface surrounding the opening, the first insulation layer side surface having a tapered shape and including an angle in relation to the surface of the conducting pad that is greater than the angle of the second insulating layer side surface;

and wherein the etching is controlled so that the first insulating layer also includes an upper surface exposed to the aperture, wherein the first insulating layer upper surface exposed to the aperture is formed substantially parallel to the surface of the pad.

110. (new) A method as in claim 109, wherein the etching is controlled so that the first insulating layer upper surface portion exposed to the aperture extends a distance of up to 3 nm between an upper end of the side surface of the first insulation layer and a lower end surface of the second insulation layer.

111. (new) A method as in claim 109, further comprising:

forming a barrier layer in the in the aperture, the barrier layer being positioned on: (1) the side surface of the second insulating layer, (2) the first insulating layer upper surface portion exposed to the aperture; and (3) the side surface of the second insulation layer; and

forming a bump electrode on the barrier layer in the opening.

112. (new) A method as in claim 109,

wherein, for the first insulating layer side surface, the angle in relation to the surface of the conducting pad is in the range of 60 degrees to 70 degrees; and

wherein, for the second insulating layer side surface, the angle in relation to the surface of the conducting pad is in the range of 30 degrees to 40 degrees.

113. (new) A method for forming a semiconductor including a bonding pad, comprising:

forming the pad;

forming a silicon oxide layer above at least the pad;

forming a silicon nitride layer above the silicon oxide layer;

forming a mask above the silicon nitride layer and providing an opening in the mask;

etching the silicon nitride layer so that a first aperture is formed in the silicon nitride layer; and

etching the silicon oxide layer so that a second aperture is formed in the silicon oxide layer;

wherein the silicon nitride layer comprises a side surface surrounding the first aperture, the silicon nitride layer side surface having a tapered shape with an angle in the range of 30 degrees to 60 degrees in relation to a surface of the pad, and the silicon oxide layer comprising a side surface surrounding the second aperture, the silicon oxide layer side surface having a tapered shape with an angle in the range of 60 degrees to 70 degrees in relation to the surface of the pad, wherein the angle of the silicon nitride layer side surface having a tapered shape is smaller than

the angle of the silicon oxide layer side surface having a tapered shape; and

wherein the etching the silicon nitride layer is controlled so as to allow the silicon oxide layer to be exposed beyond the area for the opening of the mask.